UNIVERSAL CLOCK FOR TELECOMMUNICATION APPLICATIONS

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ABSTRACT

This paper will briefly explain the synchronization scheme utilized in networks, and will present in detail the design of the **US5G,** a unique Building Integrated Time Supply (BITS) or Synchronization Supply Unit (SSU) recently developed by Gillam-FEI, a wholly owned subsidiary of Frequency Electronics, Inc. The US5G is a universal clock that is deployable in all telecom networks worldwide. We will demonstrate the advanced and exclusive characteristics of the US5G, such as its capability to accept 11 redundant input references including GPS, and deliver 40 outputs per card to the network for a total of 320 outputs, or the truly unprecedented number of 160 protected (1+1) outputs per SSU. This output density has never before been achieved by any other SSU without the use of additional expansion units. Furthermore, we will demonstrate the exclusive modular flexibility of the US5G, and it's effortlessly configurable capability to distribute synchronization to both small simple networks as well as to very large and complex global network systems. The paper will also present the process for choosing the correct Rubidium Atomic Frequency Standards and/or quartz oscillators that will best satisfy the functions of the SSU, and actual measurements of Mean Time Interval Error (MTIE) and Time Deviation (TDEV) of various employed oscillators. In addition, we will show measured data for output phase variations resulting from input reference switchover, redundant clock switchover, and output card switchover. The resulting output transients are <1 nanosecond for input reference switchover, and <6 nsec for clock and output card switchover, once again parameters never before achieved in SSUs.

1. INTRODUCTION

Today's telecommunications networks include digital switching and transmission systems. Digital switching via Time Slot Interchange (TSI) is accomplished by the rearrangement of time slots of digitized information. These time slots need to occur at the same rate. If all the time slots were created at one switch, network synchronization would not be required. However, when digital switches are connected by digital transmission systems, time slots created in one office will be switched at another office, therefore, all the offices need to be synchronized. The term synchronization, as used herein, refers to an arrangement for operating digital switching and transmission systems at a common (or synchronized) clock rate.

2. TRANSMISSION IMPAIRMENTS

Whenever differences in time exist among the Network Elements (NE) transmission errors will occur, and these errors are collectively referred to as slips. The impact to the network resulting from slips may include loss of a data frame requiring retransmission; loss of throughput when utilizing complex data and video compression techniques; missed lines in fax transmissions; and interruptions in voice communications. The purpose of a synchronization network is to avoid slips--either periodic slips due to frequency offset between the received signal and the local clock, or random slips due to phase variations such as jitter and wander. Jitter, wander and phase transients are impairments of a digital signal caused both by clocks that generate those digital signals and multiplex systems that transport those digital signals.

3. SYNCHRONIZATION METHODS

The most commonly used synchronization method is an arrangement referred to as Master/Slave. Master/Slave synchronization uses a hierarchy of clocks, and each level of the hierarchy is synchronized with reference to a higher level. The Primary Reference Clock (PRC) is a stratum 1 (ANSI) or G.811 (ITU-T) clock, and the highest quality hierarchical clock able to maintain a frequency accuracy of better than $1x10^{-11}$. PRCs are free running clocks and usually consist of an ensemble of Cesium atomic standards.

The current trend is to use Global Positioning System (GPS) as a primary synchronization source. Therefore, it is desirable to network operators to have available BITS/SSUs with embedded GPS receivers.

4. BITS/SSU

The synchronization elements installed within a network are commonly referred to as BITS, SSU or Timing Signal Generator (TSG). The major role of the SSU is to recover clocks from a reference signal and maintain timing as close as possible to the source node's timing. To achieve synch the receiver clock must perform two basic functions. First, it must reproduce the source's clock timing in the presence of impairments, and, second, it must maintain adequate timekeeping in the absence of a timing reference. The latter function is referred to as "holdover".

The ideal characteristics of a universal synchronization unit are:

- Deployable in networks operating at 1544 kbit/s and 2048 kbit/s (kHz).
- Equipped with one or two integrated GPS receivers
- Outfitted with various oscillators technologies and easily configurable to network requirements, i.e. quartz oscillator, high precision quartz oscillator, Rubidium Atomic Frequency Standards
- Equipped with sufficient number of synchronization and quality measurement input ports
- Versatile and compact mechanical packages adaptable to local requirements, i. e. unit accessible through front and/or rear panels, equipped with symmetrical or asymmetrical junctions, and adjustable impedance
- Capable of local and remote performance monitoring and management.

5. US5G UNIVERSAL BITS/SSU

Gillam-FEI has designed and produced the US5G--the world's most advanced BITS/SSU. All the ideal characteristics mentioned above have been incorporated. The US5G is shown in Figure 1, and the block diagram is depicted in Figure 2.

Input Module. The US5G is capable of simultaneously accepting 20 inputs or 10 redundant inputs for monitoring or

references as well as two GPS signals. Each input is user configurable; for example, the user can configure the impedance and choose symmetrical or asymmetrical mode. In addition, any input port is easily programmable to accept and be compliant with any one of the following signals:

- E1 (G703 section 9: 2048 kbit/s with Synch Status Message [SSM] or G703 section 13);
- DS1 (Super Frame format [SF] or Extended Super Frame format [ESF] with SSM);
- 1 MHz, 1.544 MHz, 2.048 MHz, 5 MHz, 10 MHz;
- Composite Clock (CC).

Each input is capable of monitoring an incoming signal and performing measurements such as Maximum Time Interval Error (MTIE), Time deviation (TDEV), Fractional Frequency Offset (FFOFF), drift, etc. For synch purposes the ports are redundantly configured as required by standards, and for monitoring purposes the ports are used individually.

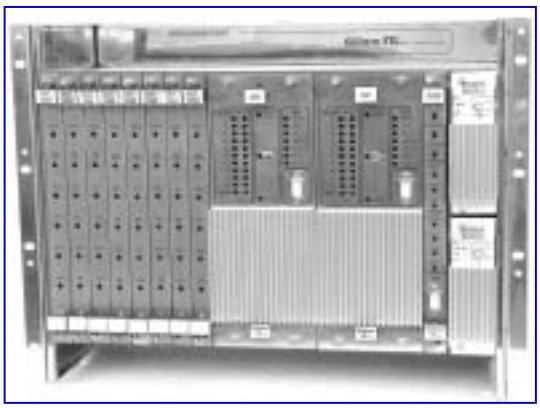

FIGURE 1. US5G

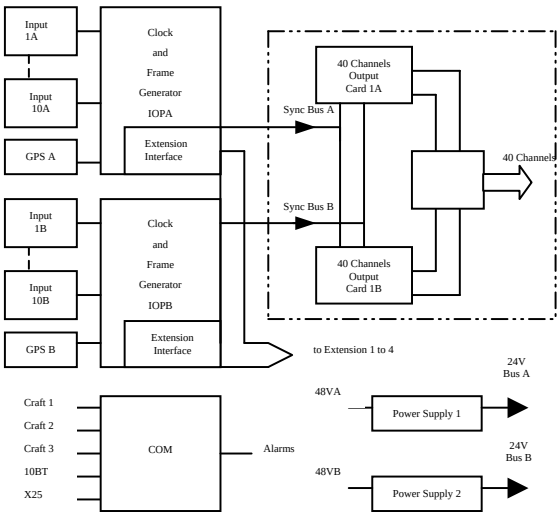

FIGURE 2. US5G Block Diagram

GPS Receiver. Two GPS receivers are integrated in the US5G. Each GPS receiver consists of two parts--the receiver itself whose output is a 100 pps signal, and a servo loop circuit that phase locks an oscillator to the 100 pps receiver output.

Clock and Frame Generator (IOP Assembly). The block diagram of the IOP card is shown in Figure 3 below. It consists of a 60 MHz fixed frequency oscillator and a GPS servo loop with a 48-bit Direct Digital Synthesizer (DDS) for correcting frequency variations. The GPS loop operates continuously irrespective of whether the GPS signal is used for synchronization purposes. The principal loop also utilizes a 48-bit DDS for frequency variations resulting in a "virtual VCXO" that is servo locked to one of the eleven available reference signals. The software is based on WIN CE.

Output Cards. The output cards are capable of being utilised in a non-redundant configuration, or in a protected 1+1 redundant configuration. There are 40 outputs per card, which allows for a maximum of 320 non-redundant outputs or 160 redundant outputs for the basic unit. Extension units (maximum 4) increase the number of outputs up to 1280 protected 1+1 redundant outputs. Output signals consist of E1/DS1 with Synch Status Message (SSM), 1 MHz, 1.544 MHz, 2.048MHz, 5MHz, 10 MHz, and Composite Clock (CC). As is the case for the input modules, output cards are configurable for various impedance and for symmetrical or asymmetrical mode.

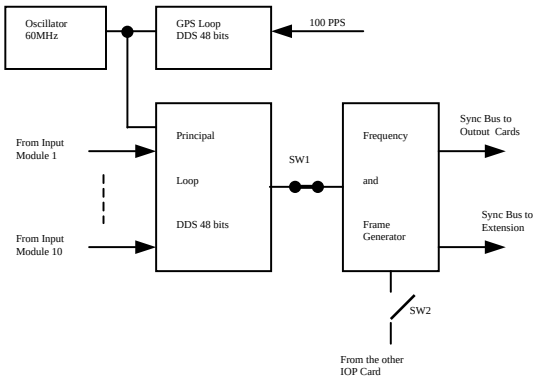

FIGURE 3. Clock and Frame Generator (IOP Assembly)

Modularity. The US5G has been designed for deployment in various types of networks. The minimum non-redundant configuration consists of one input module or one GPS receiver, a clock card, an output card and a power supply. The maximum configuration consists of 22 reference or measure inputs, and 1280 protected 1+1 redundant outputs.

6. OSCILLATOR SELECTION FOR THE US5G

The oscillator is the heart of every BITS/SSU, and redundant oscillators are normally provided to assure continuous and uninterrupted operation in the event that the selected oscillator should fail. Depending on customer requirements, all combinations of oscillator technologies are made available, for example Quartz-Quartz, Quartz-Rubidium, Rubidium-Rubidium. Three types of high quality oscillators have been chosen for the US5G. The FE-189XO cost-effective precision quartz oscillator, FE-205A high precision crystal oscillator, and FE-5680A Rubidium Atomic Frequency Standard. All the oscillators are supplied by Frequency Electronics, Inc.

The FE-189XO, double oven series, is used in over 90% of all the BITS/SSU that Gillam-FEI has supplied. The main specifications of the FE-189XO quartz oscillator are tabulated below in Table 1.

Output Frequency	4.096 MHz and 10 MHz
Frequency Stability vs. Temperature	$\pm 2 \times 10^{-10}$ (-20^{o} C to $+ 70^{o}$ C)
Aging	$\pm 1 \times 10^{-10}$ / day $\pm 3 \times 10^{-8}$ / year
Short Term Stability	5×10^{-12} for 0.1 sec
Low Phase Noise	-100dBc/Hz at 1 Hz offset -150dBc/Hz at 1 kHz offset
Standard Case and Pin-Outs	38 x 50 x 50 mm

Table 1. FE-189XO Double Oven Crystal Oscillator Specifications Highlights

The second type of oscillator used in the US5G is the FE-205A high-precision crystal oscillator. The FE-205A performance is very close to the performance of a Rubidium Atomic Frequency Standard, and it has been dubbed as the "Poor Man's Rubidium." Because of it's unique design and exceptional performance a patent has been requested and is presently pending. In particular, its temperature specifications are very impressive (Figure 4), and are especially recommended for those applications where large temperature variations are expected. The main features and performance of the FE-205A quartz oscillator are shown below.

- Most Precise Crystal Oscillator Available Today
- Large Production/High Volume
- Near Rubidium Accuracy at 1/3 the Cost
- Any frequency from 1 pps to 100 MHz
- Excellent Temperature Stability $<1x10^{-10}$
- Low Aging $<5 \times 10^{-11}$ / day; $<5 \times 10^{-8}$ /10 year
- $-40^{o}C$ to $+75^{0}C$ Operation

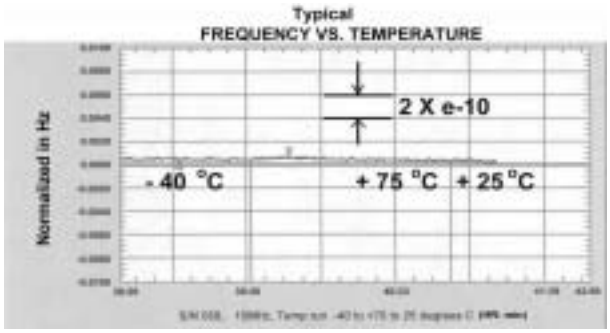

FIGURE 4. FE-205A Performance

The third type of oscillator used in the US5G is the FE-5680A Rubidium Atomic Standard. This is a low profile device, in a package less than 1 inch or 25 mm in height, and is perfectly suited for board slot mounted applications. The excellent frequency stability exhibited by the FE-5680A eliminates the need for scheduled re-calibration, and along with its small size, low power consumption, wide temperature range operation, and low cost makes the device a perfect candidate for telecommunication applications. The FE-5680A is shown in Figure 5, the main specifications are tabulated in Table 2, and a Frequency vs. Temperature plot is demonstrated in Figure 6.

FIGURE 5. FE-5680A Rubidium Atomic Frequency Standard

Output Frequency	1 Hz to 20 MHz
Frequency Stability vs. Temperature	$\pm 3 \times 10^{-10}$ (opt. $\pm 5x10^{-11}$) (-10^{o} C to + 60^{o} C)
Drift	2×10^{-11}/day (opt. $\pm 2x10^{-12}$) 2×10^{-9}/year (opt. $\pm 2x10^{-10}$)
Short Term Stability	$1.4 \times 10^{-11} / \tau^{1/2}$ (opt. $5 \times 10^{-12}/\tau^{1/2}$)
Phase Noise	-100dBc/Hz at 10 Hz offset -145dBcHz at 1000 Hz offset

Table 2. FE-5680A Rubidium Atomic Frequency Standard Specifications Highlights

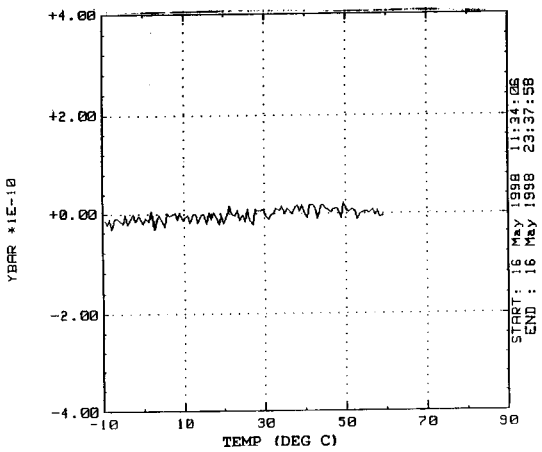

FIGURE 6. Frequency vs. Temperature, FE-5680A

Selecting the correct oscillator. Low cost, high reliability, and medium-quality behavior in holdover mode characterize quartz oscillators. Hence, quartz oscillators are best suited for those applications where the probability of switching to holdover mode is low, where the temperature variations in transmission rooms are controlled, and where the period for network restoration is short. Rubidium Atomic Standards are typically higher in cost and less reliable than quartz oscillators, but exhibit excellent behavior in holdover mode. Therefore, Rubidium devices are used when superior performance in holdover mode is essential. The FE-205A high-precision crystal oscillator or "Poor Man's Rubidium" is positioned in performance very near to a Rubidium device, but priced closer to a quartz oscillator.

The following figures demonstrate US5G performance when equipped with different oscillator types. The measurements were achieved with a PJS-2000 Portable Synchronization Network Quality Meter, which is also manufactured by Gillam-FEI. Figure 7 shows a typical TDEV, and Figure 8 shows the MTIE of an output of the US5G equipped with a Rubidium device in holdover mode.

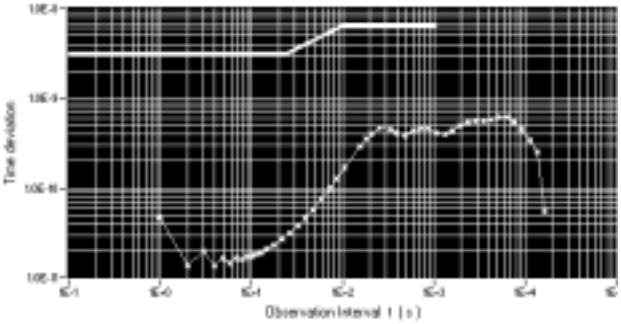

FIGURE 7. TDEV Measurement with a Quartz Oscillator in Locked Mode

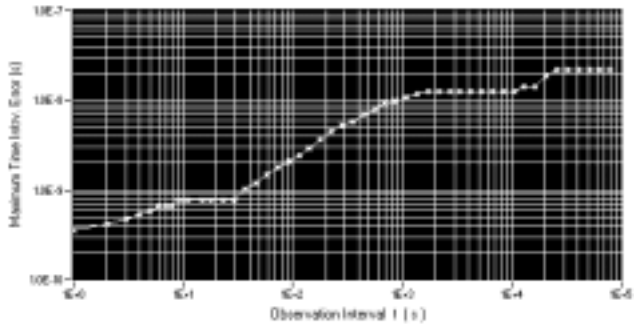

FIGURE 8. MTIE Measurement with a Rubidium Device in Holdover Mode

7. US5G PERFORMANCE DURING REFERENCE SWITCHING AND INTERNAL RECONFIGURATION

As mentioned above, redundancy is required in BITS/SSU. The unit must be capable of switching input reference signals, oscillators and associated circuits, and outputs. Furthermore, the BITS/SSU must accomplish the internal reconfiguration and reference switching with minimum phase hits to the synchronization signal. The US5G accomplishes these tasks superbly, and with minimal output disturbances. Figure 9 demonstrates the phase behavior at the output of the US5G during input reference switching. In [1], input 1 is cut and synchronization is performed on input [2]; in [2], input 2 is cut and synchronization is performed on input [3], etc. The resulting phase hit is less than 0.5 nsec.

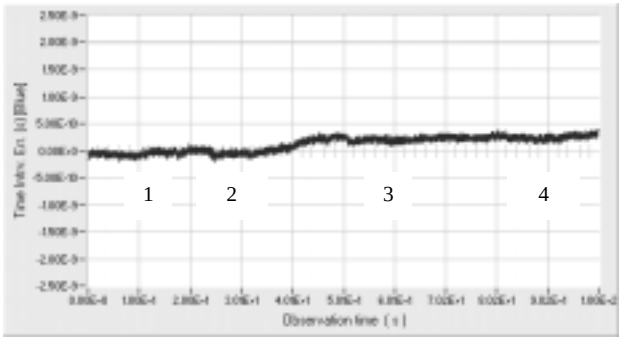

FIGURE 9. Output Phase Variation Resulting from Switching Input References

Figure 10 shows the phase behavior at the output of the US5G when the clock or IOP1 card is commuted with IOP2 card. Once again, the phase transient is extremely small and less than 4 nsec.

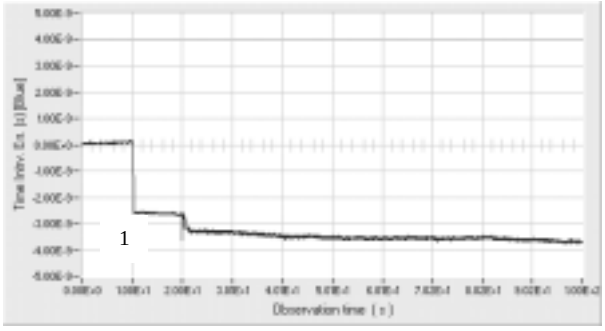

FIGURE 10. Output Phase Variation Resulting from Clock Commutations

Figure 11 shows the phase behaviour when a redundant output card is removed. The resulting phase disturbance is less than

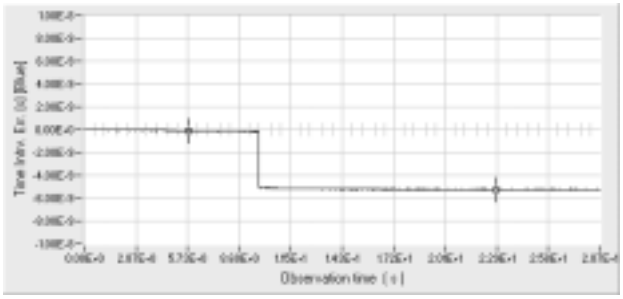

FIGURE 11 Output Phase Variation Resulting from Removal of an Output Card

8. LOCAL AND REMOTE SYNCHRONIZATION MANAGEMENT

In addition to a robust hardware design, the BITS/SSU must also be smart and capable of being monitored and managed both locally and remotely.

Management. The management of the US5G is achieved via various physical communication interfaces: a local craft port (RS232C, asynchronous serial line), two remote craft ports (RS232C, Public Switching Telephone Network [PSTN] asynchronous serial lines), a 10 Base-T Ethernet port (10 Mbps LAN access) and two X25 ports (WAN access).

Management protocol TL1. Transaction Language 1 (TL1), an ASCII man-machine management protocol defined by Bellcore—presently known as Telcordia Technologies, Inc.--is used to completely manage the US5G.

Management protocol SNMP. Simple Network Management Protocol (SNMP), a standardised Internet protocol (RFC 1157-1155), is also used to monitor and control the US5G.

Remote Synchronization Network Manager RSNM. Gillam-FEI offers a product called LYNX, which is a powerful cost effective, Remote Synchronization Network Manager (monitoring and control) based on open architecture, standards and protocols. LYNX RSNM provides remote management of the US5G, Primary Reference Clocks, other types of Time Signal Generators (TSG) and clock distribution units, as well as the management of synchronization trails in a network (nodes and links). LYNX is capable of managing over 1200 network elements, and is shown in Figure 12.

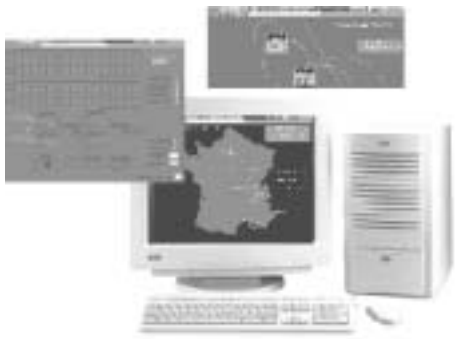

FIGURE 12. LYNX Remote Synchronisation Network Manager

9. CONCLUSION

The US5G offered by Gillam-FEI is an innovative state-of-the-art BITS/SSU that meets all the characteristics of the ideal BITS/SSU. Its novel architecture sets a new industry standard in a master shelf package that occupies minimal space. It is deployable worldwide in whatever flow of primary hierarchy used. It's designed and intended for telecom network operators to generate highly reliable synchronization signals.